

PAT-NO: JP362018040A

DOCUMENT-IDENTIFIER: JP 62018040 A

TITLE: FLATTENING OF PHOSPHOSILICATE GLASS FILM

PUBN-DATE: January 27, 1987

INVENTOR-INFORMATION:

NAME

MATSUMURA, TAKASHI

TAKEBAYASHI, TAKAMICHI

ASSIGNEE-INFORMATION:

NAME

COUNTRY

MATSUSHITA ELECTRONICS CORP

N/A

APPL-NO: JP60157264

APPL-DATE: July 17, 1985

INT-CL (IPC): H01L021/316, H01L021/88 , H01L027/08 , H01L029/78

US-CL-CURRENT: 148/DIG.133, 250/515.1 , 438/FOR.493

ABSTRACT:

PURPOSE: To shorten a channel and to flatten a phosphosilicate glass film by a method wherein PSG is heat-treated in a steam atmosphere.

CONSTITUTION: A P-type region 1 and a fixed oxide film for element isolation are formed, a polycrystalline silicon film 4 to be used as a gate electrode is formed, and the respective impurity diffusion layer 8, 9 of an N-type and a P-type are formed by the ion implantation method using a photo resist as a

mask. Then a thermal oxide film 5 is grown for 30min at 900&deg;C in an oxygen atmosphere, and a silicon nitride layer 6 is adhered at 40nm thickness. PSG 7 of 8mol% of phosphorus concentration is adhered on the upper part thereof, and flowing of PSG is performed for 90min at 900&deg;C in a steam atmosphere having 1.8 of the rate of hydrogen to oxygen, for example, in atmospheric pressure. Etching for contact holes is performed using the photo resist thereof as a mask, and Al wirings are formed finally to complete a complementary MOS semiconductor device.

COPYRIGHT: (C)1987,JPO&Japio

## PATENT ABSTRACTS OF JAPAN

(11)Publication number : 62-018040

(43)Date of publication of application : 27.01.1987

(51)Int.Cl.

H01L 21/316

H01L 21/88

H01L 27/08

H01L 29/78

(21)Application number : 60-157264

(71)Applicant : MATSUSHITA ELECTRONICS CORP

(22)Date of filing : 17.07.1985

(72)Inventor : MATSUMURA TAKASHI

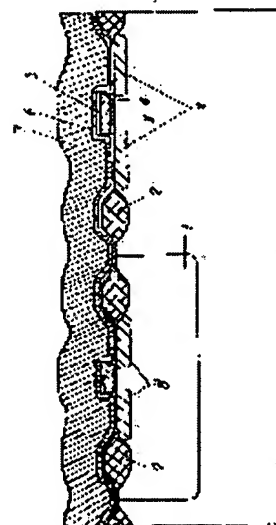
TAKEBAYASHI TAKAMICHI

## (54) FLATTENING OF PHOSPHOSILICATE GLASS FILM

## (57)Abstract:

PURPOSE: To shorten a channel and to flatten a phosphosilicate glass film by a method wherein PSG is heat-treated in a steam atmosphere.

CONSTITUTION: A P-type region 1 and a fixed oxide film for element isolation are formed, a polycrystalline silicon film 4 to be used as a gate electrode is formed, and the respective impurity diffusion layer 8, 9 of an N-type and a P-type are formed by the ion implantation method using a photo resist as a mask. Then a thermal oxide film 5 is grown for 30min at 900°C in an oxygen atmosphere, and a silicon nitride layer 6 is adhered at 40nm thickness. PSG 7 of 8mol% of phosphorus concentration is adhered on the upper part thereof, and flowing of PSG is performed for 90min at 900°C in a steam atmosphere having 1.8 of the rate of hydrogen to oxygen, for example, in atmospheric pressure. Etching for contact holes is performed using the photo resist thereof as a mask, and Al wirings are formed finally to complete a complementary MOS semiconductor device.



## LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision, of rejection]

[Kind of final disposal of application other than the  
examiner's decision of rejection or application  
converted registration]

[Date of final disposal for application]